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A Threshold Voltage Compensated Wideband RF Energy Harvesting Rectifier at 45 nm Technology

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***Abstract*— Equipping a modern day communication system with RF energy harvesting capability is the need of the hour and to make this a reality a high frequency rectifier is indeed indispensable. To trap the real RF energy successfully the rectifier must be able to provide a sufficiently higher percentage conversion ratio (PCE) at a lower range of signal power. This paper presents a simplified 3-transistor design of a high frequency rectifier with a threshold voltage compensation techniques to achieve a PCE upto 85% at -2dBm in its single stage implementation. This can be stated to be one of the highest in-class efficiency as compared to recently reported designs. From the frequency response it is observed to exhibit wide band performance spanning almost all popular wireless bands. The dynamic power dissipation (DPD) is calculated to be 6.25pW at -2dB, whereas the leakage power (LP) is observed to be zero.**

Keywords—Energy Harvesting, PCE, Transmission Gate, Dynamic Power Dissipation, Leakage Power

I. INTRODUCTION

Upcoming communication networks are increasingly focussing on energy harvesting as an option for self-sustaining operation in physical and virtual modes [1]. Lately, artificial means are receiving greater importance in providing support towards energy harvesting applications. In this regard, network topology, deployment and device design play important roles [1][2][3].

A rectifier or charge pump is undoubtedly the primary part of the energy harvester design. There are several design challenges in the design of a rectifier. A few of them are wide frequency compatibility, low power dissipation, lesser silicon area etc. But to have a higher value of the power conversion efficiency (PCE) at lower input power is the most important criteria which the designer must address while formulating an efficient circuit design. Cross coupled bridge configuration with differential RF input can be designed which give low on state current and small leakage current and thereby offering better PCE[4]. Voltage doubler Ultra High Frequency (UHF) rectification unit is also designed with the technique of internal cancellation to achieve a zero-threshold transistor and thereby an accepted PCE is achieved with reduced area [5]. Dickson charge pump is one of the most widely used structures for this purpose and different modifications have been presented by several designers for specific applications and efficiencies. The Dickson charge pump has been modified to reduce the leakage current with linear regulator and thereby total power consumption can be reduced [6]. Rectifier based on improved Dickson charge pump in two configurations are presented which works in GSM band with a satisfactory PCE [7]. Also dynamic threshold reduction technique based CMOS rectifier has been designed with the use of a clamper to reduce the effective threshold voltage and increase the sensitivity and hence achieving a high PCE [8].

This paper presents a simplified 3-transistor design of a high frequency rectifier with a threshold voltage compensation technique to achieve a PCE upto 85% at -2dBm in its single stage implementation. It is found to be one of the highest in-class efficiency as compared to recently reported designs. From the frequency response it is observed to exhibit wide band performance spanning almost all popular wireless bands. The dynamic power dissipation (DPD) is calculated to be 6.25pW at -2dB, whereas the leakage power (LP) is observed to be zero.

The remaining of the paper is organised as follows. Section II deals with the proposed design with explanation of the functionality, Section III deals with simulation results and discussion and Section IV includes the concluding remark.

II. THE PROPOSED 3-TRANSTOR DESIGN

The basic functionality of the proposed design is based on the idea of a transmission gate (TG). The TG is used in many CMOS based circuits. The nMOS pass transistor can pass the negative voltage efficiently with less propagation time while the pMOS pass transistor allows the positive voltage efficiently with less propagation time; hence transmission can be a solution to such situations where the circuit is meant to deal with both the voltage levels. Also the TG generates a sufficiently higher on state current for a wide range of input voltages.

The design presented here can be said to be a simplification to the TG based rectifier reported in [9]. When the input voltage is positive, the nMOS in the TG will allow the current to flow through and when the input is negative the pMOS in the TG makes an open path for the current to flow. The current generated in both the cases will flow through the diode connected nMOS at the output stage making an unidirectional current flow to the output capacitor. Thus the rectified output voltage may be collected across the capacitor. But the output generated yields lower PCE because the transistors do not remain in the active states as the value of the input signal falls below threshold voltage value of the transistor. Hence some compensation techniques is required. A simple threshold voltage compensation technique is proposed here with the use of a capacitor at the gate of each transistors as shown in Fig. 1. This will allow the capacitor to retain some charge at every cycle and thereby add up a voltage to the gate at every subsequent cycle. This will effectively compensate the threshold voltage and allow the circuit to operate at a wider time period which will in turn enhance

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